REMARKS

Claims 1 - 10 are pending in the application. By this Amendment, claims 3, 5, 6 and 7 are amended and claim 10 is added. Claims 8 and 9 stand withdrawn from consideration.

Claim 1 is rejected under 35 USC 102 (b) as anticipated by U. S. Patent No. 5,587,337 to Idaka et al. The rejection is respectfully traversed.

Idaka discloses a semiconductor device for use in a TAB mounting technique. In this device, a LSI chip 1 is covered with a passivation film 13 which has an opening 13a where a pad 12 of aluminum is exposed. A bump electrode 3 made of gold, for example, is provided so as to cover the opening 13a. It is also disclosed that the bump electrode 3 may be formed by way of gold plating.

Claim 1 is directed to a semiconductor chip that includes a surface protective film for covering internal wiring, an external connection pad and a wire connecting portion. Claim 1 recites that the external connection pad is formed by partially exposing the internal wiring from the surface protective film. Claim 1 also recites that the wire connecting portion is formed using a metal material having oxidation resistance on the external connection pad and to which a wire for electrical connection to an external terminal is connected.

It is respectfully submitted that the rejection is improper because the applied art fails to teach each element of claim 1. Particularly, the applied art fails to teach a wire connecting portion which is formed on the external connection pad and to which a wire for electrical connection to an external terminal is connected. In other words, the bump 3 in Idaka the is not one to which a bonding wire is to be bonded. As a result, claim 1 is allowable over the applied art.

Withdrawal of the rejection is respectfully requested.

Claims 2, 3 and 4 are rejected under 35 USC 103 (a) as unpatentable over Idaka as applied to claim 1 and further in view of U. S. Patent No. 5,734,199 to Kawakita et al. The rejection is respectfully traversed.

As discussed above, claim 1 is allowable over Idaka. Kawakita fails to cure the

deficiencies Idaka. Thus, claim 1 is allowable over the combination of the applied art.

Claims 2, 3 and 4 depend from claim 1 and include all the features of claim 1. Thus, the dependent claims are allowable at least for the reasons claim 1 is allowable as well as for the features they recite.

Withdrawal of the rejection is respectfully requested.

Claim 5 is rejected under 35 USC 103 (a) as unpatentable over Idaka as applied to claim 1 above and further in view of U. S. Patent No. 6,060, 768 to Hayashida et al. The rejection is respectfully traversed.

As discussed above, claim 1 is allowable over Idaka. Hayashida fails to cure the deficiencies of Idaka. Thus, claim 1 is allowable over the combination of the references.

Claim 5 depends from claim 1 and include all of the features of claim 1. Claim 5 is therefore allowable at least for the reasons claim 1 is allowable as well as for the features it recites.

Withdrawal of the rejection is respectfully requested.

Claims 6 and 7 are rejected under 35 USC 103 (a) as unpatentable over Kawakita in view of Hayashida. The rejection is respectfully traversed.

Kawakita discloses a semiconductor device of the chip-on-chip structure that has a first and second semiconductor chips 110 and 120. Bumps 113 and 123 are provided on the first and second semiconductor chips 110 and 120, respectively, which are joined together to establish electrical connection between the first and second semiconductor chips 110 and 120. The second semiconductor chip 120 is larger than the first semiconductor chip 110, and therefore, the second semiconductor chip 110 has a region that is not covered by the first semiconductor chip 110. In this region on the second semiconductor chip 120, testing electrodes 121 are provided. The bumps 124 are provided as covering the testing electrodes 121.

The bumps 124 are not for a wire bonding connection but for use in the testing of the semiconductor chips 110 and 120 by means of a testing probe to be pressed against the bump 124.

Hayashida discloses a process to form a gold plating layer on the portion where a wire 8 is to be bonded.

Claim 6 is directed to a semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a surface of the primary chip. Claim 6 recites that the primary chip includes a surface protective film for covering internal wiring, an external connection pad, a wire connecting portion, an internal connection pad and an electrical contact projection. Claim 6 recites that the external connection pad is formed by partially exposing the internal wiring from the surface protective film. Claim 6 also recites that the wire connecting portion is formed using a metal material having oxidation resistance on the external connection pad and to which a wire for electrical connection to an external terminal is connected. Claim 6 also recites that the internal connection pad is formed by partially exposing the internal wiring from the surface protective film in a portion that different from the external connection pad. Furthermore, claim 6 recites that the electrical contact projection is formed in a raised state on the internal connection pad using a metal material having oxidation resistance for electrically connecting the primary chip and the secondary chip.

It is respectfully submitted that none of the applied art, alone or in combination, teaches or suggests the features of claim 6. Specifically, none of the applied art teaches or suggests a wire connecting portion formed on an external connection pad to which a wire for electrical connection to an external terminal is connected. In short, the bump 124 of Kawakita is not for use in wire bonding. At least for these reasons, claim 6 is allowable over the applied art.

Claim 7 depends from claim 6 and Includes all of the features of claim 6. Thus, claim 7 is allowable at least for the reasons claim 6 is allowable as well as for the features it recites.

Withdrawal of the rejection is respectfully requested.

Newly-added claim 10 also includes features not shown in the applied art. Allowance of claim 10 is respectfully solicited.

In view of the foregoing, reconsideration of the application and allowance of the

pending claims are respectfully requested. Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

Please charge any fee deficiency or credit any over payment to Deposit Account No.18-0013 that is necessary to consider an appropriate response timely filed.

Respectfully submitted,

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Enclosure(s): Marked-Up Version of Amended Claims

MARKED-UP VERSION OF AMENDED CLAIMS

3. (Amended) The semiconductor chip according to claim 2, further comprising

an internal connection pad which is formed by partially exposing said the internal wiring from said surface protective film in a portion of different from said external connection pad, and

[a bump] an electrical contact projection formed in a raised state on the internal connection pad using a metal material having oxidation resistance in order to make electrical connection to the said solid device.

5. (Amended) The semiconductor chip according to claim [1] 3, wherein

said wire connecting portion is composed of the same material as that for said [bump] electrical contact projection.

6. (Amended) A semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a surface of a primary chip, wherein

said primary chip comprises

a surface protective film for covering internal wiring,

an external connection pad formed by partially exposing the internal wiring from the surface protective film,

a wire connecting portion which is formed using a metal material having oxidation resistance on the external connection pad and to which a wire for electrical connection to an external terminal is connected,

an internal connection pad which is formed by partially exposing said internal wiring from said surface protective film in a portion different from said external connection pad, and

[a bump] an electrical contact projection which is formed in a raised state on the internal connection pad using a metal material having oxidation resistance for electrically connecting the primary chip and the secondary chip.

7. (Amended) The semiconductor chip according to claim 6, wherein said wire connecting portion is composed of the same material as that for said [bump] electrical contact projection.

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